

1 Amendments to the Claims:

2       This listing of claims will replace all prior versions, and  
3 listings, of claims in the application using (Original) (Currently  
4 Amended) (New) (Canceled) (Previously Presented) nomenclature, as  
5 recited in the below listing of claims.

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7 1. (Previously Presented) A timing recovery loop for generating  
8 adjusted timing pulses from a baseband signal waveform encoding a  
9 self clocking digital bit stream, the timing recovery loop  
10 comprising,

11       a pulse detector for generating data transition pulses from the  
12 baseband signal waveform, the pulse detector for comparing the data  
13 transition pulses with the adjusted timing pulses for generating  
14 early signals and lag signals,

15       a random walk counter for counting the early signals and lag  
16 signals for generating a running count,

17       a threshold comparator for determining when the running count  
18 exceeds a predetermined threshold value, and

19       a timing pulse delay adjustor for adjusting an adjusted timing  
20 pulse delay communicated to the pulse detector for delaying the  
21 adjusted timing pulses for synchronizing the adjusted timing pulses  
22 with the data transition pulses when the running count exceeds the  
23 predetermined threshold value.

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1 2. (Original) The timing recovery loop of claim 1 further  
2 comprising,

3 a data detector for generating a reconstructed digital bit  
4 stream by sampling the baseband signal waveform by the adjusted  
5 timing pulses.

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8 3. (Original) The timing recovery loop of claim 1 further  
9 comprising,

10 a threshold value selector for selecting the threshold value.

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13 4. (Original) The timing recovery loop of claim 1 further  
14 comprising,

15 a threshold value selector for selecting the threshold value,  
16 and

17 an adaptive means for monitoring the rate at which the timing  
18 pulse delay is adjusted, the threshold value selector adaptively  
19 selecting different threshold values when the adjustment rate  
20 exceeds a predetermined rate.

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1 5. (Original) The timing recovery loop of claim 1 further  
2 comprising,

3 a count magnitude generator for generating the magnitude count  
4 from the running count, the magnitude count being fed to the  
5 threshold comparator for determining when the running count exceeds  
6 the predetermined threshold value, and

7 a count sign clipper for generating a count sign from the  
8 running count, the count sign being fed to the timing pulse delay  
9 adjustor for generating a timing pulse delay to adjust the adjusted  
10 timing pulses, the sign count for increasing the timing pulse delay  
11 when the data transition pulses arrive late relative to the  
12 adjusted timing pulses and for decreasing the timing pulse delay  
13 when the data transition pulses arrive early relative to the  
14 adjusted timing pulses.

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17 6. (Original) The timing recovery loop of claim 1 wherein the pulse  
18 detector comprises,

19 a data transition pulse generator for generating the data  
20 transition pulses,

21 a timing delay for delaying reference timing pulses into the  
22 adjusted timing pulses, and

23 a lead and lag generator for generating lead and lag signals  
24 for early and late arrivals of the data transition pulses relative  
25 to the adjusted timing pulses.

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1 7. (Original) The timing recovery loop of claim 1 wherein the pulse  
2 detector comprises,  
3 a data transition pulse generator for generating the data  
4 transition pulses,  
5 a timing delay for delaying reference timing pulses into the  
6 adjusted timing pulses, and  
7 a data transition pulse counter for counting the number of  
8 data transition pulses within a search window following an adjusted  
9 timing pulse, and  
10 a lead and lag generator for generating lead and lag signals  
11 for early and late arrivals of the data transition pulses relative  
12 to the adjusted timing pulses when one and only one data transition  
13 pulse occurs within each search window following an adjusted timing  
14 pulse.

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1 8. (Original) The timing recovery loop of claim 1 wherein the pulse  
2 detector comprises,

3 a data transition pulse generator for generating the data  
4 transition pulses,

5 a window delay for delaying the data transition pulses by half  
6 of a search window to center the data transition pulses within  
7 respective search windows,

8 a timing delay for delaying by a timing pulse delay the  
9 reference timing pulses into the adjusted timing pulses, the timing  
10 pulse delay being generated by the timing delay adjustor, the  
11 timing pulse delay being adjusted when the running count exceeds  
12 predetermined threshold value,

13 a data transition pulse counter for counting the number of  
14 data transition pulses within the search window following an  
15 adjusted timing pulse, and

16 a lead and lag generator for generating lead and lag signals  
17 for early and late arrivals of the data transition pulses relative  
18 to the adjusted timing pulses when one and only one data transition  
19 pulse occurs within a respective one of the search windows  
20 following a respective one of the adjusted timing pulses.

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24 9. (New) The timing recovery loop of claim 1, wherein,

25 the random walk counter sums the lead signals and lag signals as  
26 the running count.

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